MGA-61563

# Avago Technologies MGA-61563 Current-Adjustable Low Noise Amplifier

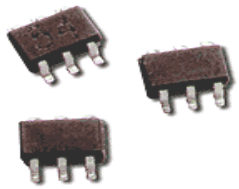
## Description

This E-pHEMT RFIC is an easy-to-use high linearity low noise amplifier built-in with Smart Bias function. For Smart Bias function, one external resistor is used to set the bias current taken by the device over a wide range. This allows the designer to use the same part in several circuit positions and tailor the linearity performance and current consumption to suit each position.

It is ideal as a LNA or driver amplifier for Cellular/PCS/W-CDMA base stations, WLL, Fixed Wireless Access, Wireless LAN and other high performance applications in the 0.1 to 6 GHz frequency range.

Lead (PB) Free
RoHS 6 fully compliant

**Lifecycle status:** Active



## Features

Typical performance at 2 GHz 3V/42mA is NF=1.4dB, OIP3=28dBm, P1dB=15dBm and Ga=16.5dB.

# MGA-61563
Current-Adjustable, Low Noise Amplifier

## Data Sheet

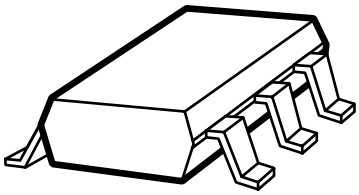
### Description

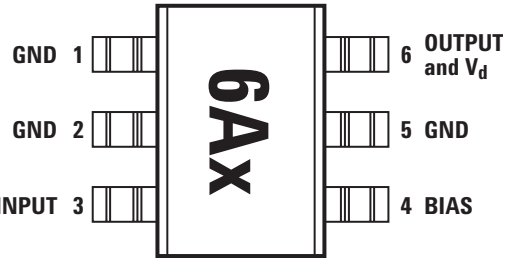
Avago Technologies' MGA-61563 is an economical, easy-to-use GaAs MMIC amplifier that offers excellent linearity and low noise figure for applications from 0.1 to 6 GHz. Packaged in an miniature SOT-363 package, it requires half the board space of a SOT-143 package.

One external resistor is used to set the bias current taken by the device over a wide range. This allows the designer to use the same part in several circuit positions and tailor the linearity performance (and current consumption) to suit each position. The MGA-61563 is normally operating with Id set in the 20-60mA range

The output of the amplifier is matched to 50Ω (below 2:1 VSWR) across the entire bandwidth and only requires minimum input matching. The amplifier allows a wide dynamic range by offering a 1.2 dB NF coupled with a +28.5 dBm Output IP3. The circuit uses state-of-the-art E-pHEMT technology with proven reliability. On-chip bias circuitry allows operation from a single +3V or +5V power supply, while internal feedback ensures stability (K>1) over all frequencies.

### Pin Connections and Package Marking






Note:
Package marking provides orientation and identification:
"6A" = Device Code
"x" = Date code indicates the month of manufacture.

### Features

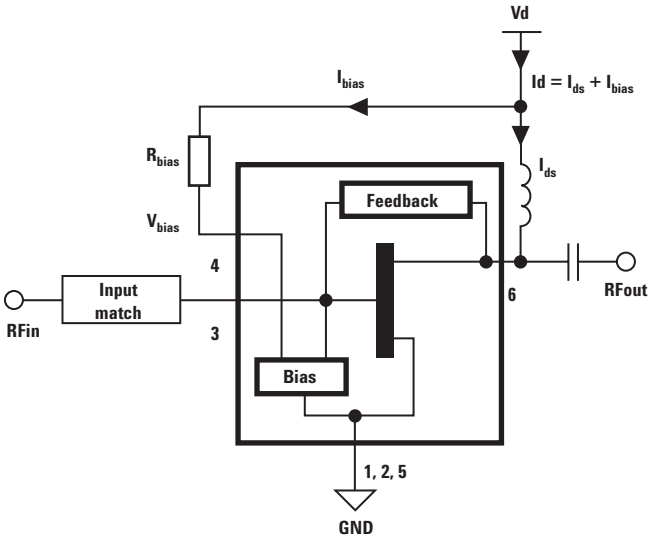
- Single +3V or + 5V supply
- High linearity
- Low noise figure
- Miniature SOT363 (SC70) package
- Unconditionally stable
- Lead-free option available

### Specifications at 2 GHz; 3V, 41 mA (Typ.)

- 28.5 dBm OIP3
- 1.2 dB noise figure
- 16.6 dB gain
- 15.8 dBm $P_{1dB}$

**Attention: Observe precautions for handling electrostatic sensitive devices.**
ESD Machine Model (Class A)
ESD Human Body Model (Class 0)
*Refer to Avago Technologies Application Note A004R: Electrostatic Discharge Damage and Control.*

## Simplified Schematic




## MGA-61563 Absolute Maximum Ratings[1]

| Symbol | Parameter | Units | Absolute Maximum |
|---|---|---|---|
| $V_d$ | Device Voltage (pin 6)[2] | V | 6 |
| $I_d$ | Device Current (pin 6)[2] | mA | 100 |
| $P_{in}$ | CW RF Input Power (pin 3)[3] | dBm | 18 |
| $I_{ref}$ | Bias Reference Current (pin 4) | mA | 10 |
| $P_{diss}$ | Total Power Dissipation[4] | mW | 500 |
| $T_{CH}$ | Channel Temperature | °C | 150 |
| $T_{STG}$ | Storage Temperature | °C | 150 |
| $\theta_{ch\_b}$ | Thermal Resistance[5] | °C/W | 115 |

Notes:
1. Operation of this device in excess of any one of these parameters may cause permanent damage.
2. Assumes DC quiescent conditions.
3. With the DC (typical bias) and RF applied to the device at board temperature $T_B$ = 25°C.
4. Total dissipation power is referred to lead "x" temperature. Tc=92.5°C, derate Pdiss at 8.7mW/°C for Tc>92.5°C.
5. Thermal resistance measured using 150°C Liquid Crystal Measurement method.

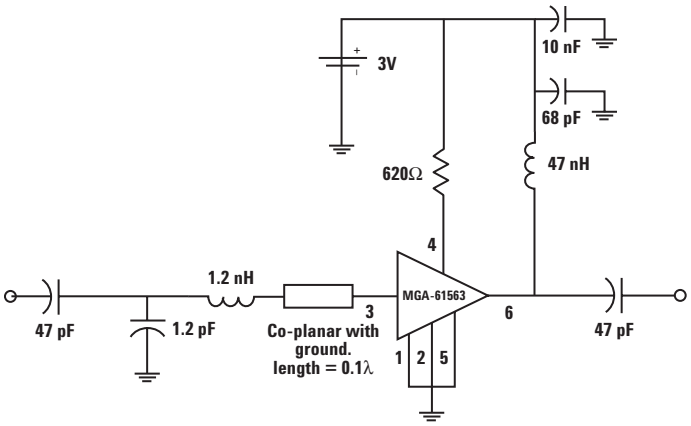



**Figure 1. Test circuit of the 2 GHz production test board used for NF, Gain and OIP3 measurements. This circuit achieves a trade-off between optimal NF, Gain, OIP3 and input return loss. Circuit losses have been de-embedded from actual measurements.**

## MGA-61563 Electrical Specifications

Rbias = 620ohm
TC = 25°C, ZO = 50Ω, Vd = 3V (unless otherwise specified)

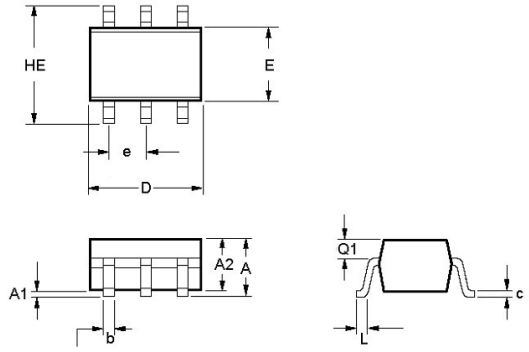
| Symbol | Parameters and Test Conditions | Freq | Units | Min. | Typ. | Max. | Std Dev |
|---|---|---|---|---|---|---|---|
| Id[1,2] | Device Current | | mA | 32 | 41 | 48 | 0.91 |
| $NF_{test}$[1,2] | Noise Figure in test circuit [1] | f = 2.047 GHz | dB | | 1.17 | 1.8 | 0.03 |
| $G_{test}$[1,2] | Associated Gain in test circuit[1] | f = 2.047 GHz | dB | 15 | 16.6 | 18 | 0.36 |
| $OIP3_{test}$[1,2] | Ouput 3rd Order Intercept in test circuit[1] | f = 2 GHz | dBm | 26 | 28.5 | | 0.5 |
| $NF_{50\Omega}$[3] | Noise Figure in 50Ω system | f = 0.2 GHz | dB | | 1.4 | | |
| | | f = 0.5 GHz | | | 1.1 | | |
| | | f = 1.0 GHz | | | 0.9 | | |
| | | f = 2.0 GHz | | | 1.0 | | 0.03 |
| | | f = 3.0 GHz | | | 1.4 | | |
| | | f = 4.0 GHz | | | 1.8 | | |
| | | f = 5.0 GHz | | | 2.3 | | |
| | | f = 6.0 GHz | | | 2.7 | | |
| $\|S_{21}\|^2$ [3] | Associated Gain in 50Ω system | f = 0.2 GHz | dB | | 21 | | |
| | | f = 0.5 GHz | | | 20 | | |
| | | f = 1.0 GHz | | | 19.3 | | |
| | | f = 2.0 GHz | | | 15.5 | | 0.36 |
| | | f = 3.0 GHz | | | 12.4 | | |
| | | f = 4.0 GHz | | | 10.4 | | |
| | | f = 5.0 GHz | | | 8 | | |
| | | f = 6.0 GHz | | | 6.9 | | |
| $OIP3_{50\Omega}$[3] | Output 3rd Order Intercept Point in 50Ω system | f = 0.2 GHz | dBm | | 29 | | |
| | | f = 0.5 GHz | | | 29.8 | | |
| | | f = 1.0 GHz | | | 30.5 | | |
| | | f = 2.0 GHz | | | 31.7 | | 0.5 |
| | | f = 3.0 GHz | | | 30.9 | | |
| | | f = 4.0 GHz | | | 30.6 | | |
| | | f = 5.0 GHz | | | 30.6 | | |
| | | f = 6.0 GHz | | | 30.7 | | |
| $P1dB_{50\Omega}$[3] | Output Power at 1dB Gain Compression in 50Ω system | | f = 0.2 GHz | | dBm | | 15.6 |
| | | f = 0.5 GHz | | | 15.5 | | |
| | | f = 1.0 GHz | | | 15.4 | | |
| | | f = 2.0 GHz | | | 15.1 | | |
| | | f = 3.0 GHz | | | 15.1 | | |
| | | f = 4.0 GHz | | | 14.8 | | |
| | | f = 5.0 GHz | | | 14.6 | | |
| | | f = 6.0 GHz | | | 14.6 | | |

Notes:
1. Guaranteed specifications are 100% tested in the production test circuit as shown in Figure 1, the typical value is based on measurement of at least 500 parts from three non-consecutive wafer lots during initial characterization of this product.
2. Circuit achieved a trade-off between optimal NF, Gain, OIP3 and input return loss.
3. Parameter quoted at 50Ω is based on measurement of selected typical parts tested on a 50Ω input and output test fixture.

## Ordering Information

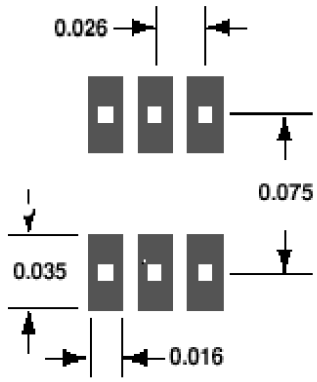
| Part Number | No. of Devices | Container |
|---|---|---|
| MGA-61563-TR1G | 3000 | 7" Reel |
| MGA-61563-TR2G | 10000 | 13" Reel |
| MGA-61563-BLKG | 100 | antistatic bag |

## SOT-363/SC-70 (JEDEC DFP-N) Package Dimensions



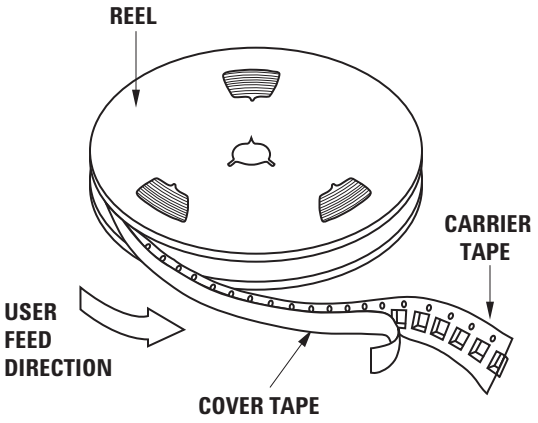

| Dimensions | | |
|---|---|---|
| **Symbol** | **Min (mm)** | **Max (mm)** |
| E | 1.15 | 1.35 |
| D | 1.80 | 2.25 |
| HE | 1.80 | 2.40 |
| A | 0.80 | 1.10 |
| A2 | 0.80 | 1.00 |
| A1 | 0.00 | 0.10 |
| e | 0.650 BCS | 0.650 BCS |
| b | 0.15 | 0.30 |
| c | 0.10 | 0.20 |
| L | 0.10 | 0.30 |

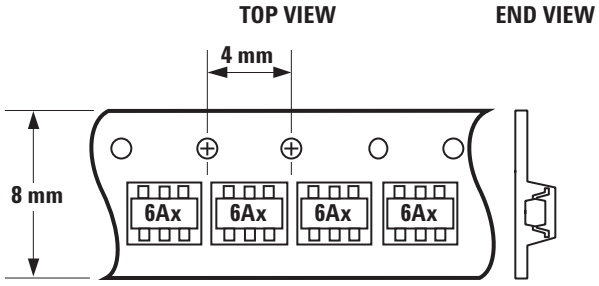
## Recommended PCB Pad Layout for Agilent's SC70 6L/SOT-363 Products




(dimensions in inches)

## Device Orientation




(Package marking example orientation shown.)